Application No. 10/790,403
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REMARKS

Claims 1-31 are currently pending. Claims 1-12 and claims 27-31 have been withdrawn from prosecution. Claims 13-23 have been allowed. Claims 24-26 stand rejected under 35 U.S.C. § 112, second paragraph and §103(a).

The Applicants respectfully request reconsideration of the pending application for the following reasons. Withdrawal of the same is respectfully requested.

35 U.S.C § 103(a) REJECTIONS

Claims 24-26 stand rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent Application Publication Number 2001/0032977 to Abe, et al. ("Abe") in view of U.S. Patent Number 6,335,231 to Yamazaki, et al. ("Yamazaki"). More specifically, per the Examiner, Abe otherwise anticipates the invention as claimed but for the (first) "heating step to a cleaving temperature", by which the silicon surface of the second body is bonded to the silicon dioxide layer of the first body "by heating the hydrogen implanted body" of the silicon surface. Moreover, per the Examiner, it would have been obvious to combine Abe with Yamazaki's method of fabricating a SOI substrate in which two silicon wafers are bonded by first heating the wafers to a temperature to cause cleavage and by then heating the wafers to a higher temperature strengthen the bond therebetween. The Applicants respectfully traverse these rejections for the following reasons.

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The "smart cut method" disclosed by Abe in para. [0058]-[0064] and shown in FIG 9 comprises one or more cycles of following three steps:

(a) implanting hydrogen ions into a bond wafer (18) at a desired depth in a wafer (18) that includes an oxide film (A) while the temperature of the wafer (18) "is maintained lower than a temperature which a gas produced by the ion implantation can emit from the semiconductor through diffusion;"

(b) contacting and bonding the silicon oxide of the semiconductor bond wafer (18) to a reinforcing base wafer (16) at room temperature; and

(c) heat treating the bond wafer (18) and base wafer (16) to "a temperature higher than the temperature of the ion bombardment and suitable for separating (splitting, destacking) the thin film and the substrate bulk".

Thus, according to Abe, initially, hydrogen ions are implanted in the silicon body having a silicon oxide layer (i.e., the bond wafer) and bonding occurs at room temperature. In contrast, according to claim 1, initially, hydrogen ions are implanted only in the silicon body (i.e., the base wafer), which is then bonded to a silicon dioxide layer of a separate the silicon body at an elevated temperature. Thus, not only does Abe not teach bonding at an elevated temperature, but it also teaches initially implanting hydrogen ions in the bond wafer rather than in the base wafer (as presently claimed).

Yamazaki addresses shortcomings with respect to "the smart-cut method", see, e.g., Yamazaki, col. 1, lines 56-60, disclosing improving the "smart-cut method" by using a "single crystal semiconductor substrate having a main surface of a {110} plane in

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contact with an insulating layer." Id., col. 3, lines 28-30. Per Yamazaki, the {110} plane of a single crystal silicon layer "has not been conventionally used before." Indeed,

> **first priority is given to adhesion of a single crystal silicon layer** to an under layer (silicon oxide layer) in the SOI substrate, and the invention is characterized by **using the single crystal silicon substrate having the crystal face of then [sic: the] {110} plane which has not been conventionally used before**. That is, the invention is characterized by having the single crystal semiconductor substrate having the main surface (crystal face) of the {110} plane as a material. **The SOI technique, such as SIMOX, ELTRAN, or Smart-Cut is, fully used**, so that a SOI substrate with high reliability is formed. Incidentally, an oriental flat of the single crystal semiconductor substrate having the main surface of the {110} plane may be made a {110} plane.

Id., col. 4, lines 45-61 (Emphasis added).

Referring to Yamazaki FIG. 1A to 1F and the related disclosure, Yamazaki teaches bonding silicon substrates (101 and 104) that each have silicon oxide layers (102 and 105, respectively), to form a silicon oxide-to-silicon oxide interface. See, e.g., Id., col. 6, line 1-15, FIG. 1C, and FIG. 1D. One of the substrates has a hydrogen layer in the non-insulating silicon region. The whole is then subjected to a first heating treatment to facilitate separation of the single crystal silicon at the hydrogen boundary and to a second, annealing heat treatment that bonds the single crystal silicon (101) to the silicon substrate (104) and that provides an insulating layer (107, formerly the silicon oxide layer 105). See, e.g., Id., col. 6, lines 16-31.

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More particularly, the present invention bonds the silicon oxide layer of a bond wafer to a silicon base wafer that has been ion bombarded. Abe bonds a silicon oxide layer of a bond wafer that has been ion bombarded to a silicon base wafer that has not. Yamazaki bonds a silicon oxide layer to a silicon oxide layer, one on the bond wafer and one on the base wafer. These constitute substantially different method steps with different results. None of the art cited by the Examiner teaches taking each process of the art apart

In conclusion, Abe teaches the "smart-cut" method and Yamazaki teaches an improvement thereto. For the reasons provided above, neither Abe nor Yamazaki teaches, mentions or suggests the method as claimed by the present invention. Because Yamazaki, like the present invention, is itself an improvement to the method disclosed in Abe, it teaches a method that is distinguishable from that in claim 1.

Accordingly, the Applicants believe that claims 24-26 are not made obvious by Abe in view of Yamazaki and, further, satisfy all of the requirements of 35 U.S.C. §§ 101, et seq., especially § 103(a). As such, the claims are in condition for allowance.

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The Examiner is encouraged to telephone the undersigned attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

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